Université Polytechnique HAUTS-DE-FRANCE

Embedded systems reliability

Composante
INSA Hauts-de-France

Présentation

Description

Cours :
Chapter I: Background
1. Processing Systems Families
2. Microprocessor, from code to execution
3. FPGA Architecture
4. CMOS Circuit design
4.1. Memories
4.2. Combinational Elements
5. Reliability-related Definitions
Chapter II: Errors & Degradations Mechanisms
1. Aging-related degradation mechanisms
2. Soft Errors
3. Masking Phenomena
4. AVF and reliability models (SER)
5. Fault injection mechanisms
Chapter III: Reliability Enhancement Techniques
1. Reliability Enhancement of SRAM memories
2. Reliability Enhancement of Processing Elements
3. Reliability Enhancement of Multiprocessor System On Chip (MPSoCs)
TD : Reliability assessment of components and devices.
TP : Reliability assessment of a CPU based on fault injection in a simulation platform (SimpleScalar / Sniper …)

Infos pratiques

Lieu(x)

> CAMPUS MONT HOUY - VALENCIENNES